

1 Page 89, line 18, replace "now allowed" with --now U.S. Patent  
2 No. 5,539,775--.

3 Page 137, line 23, after "as inventors," insert --now U.S. Patent  
4 No. 5,480,834--.

5 Page 185, line 2, change "show" to --shown--.

6 Page 188, line 20, after "diagram" insert --(see Figs. 69 and 70)--.

7  
8 In the Claims

9 Cancel claims 1-252 in favor of new claims as follows.

10  
11 ~~--253.~~ An amplifier configured to be powered by a selectively  
12 engageable voltage source, the amplifier comprising:

13 a differential amplifier having first and second inputs for receiving  
14 an input signal to be amplified, and having an output;

15 first resistances between the voltage source and respective inputs  
16 of the differential amplifier; and

17 second, selectively engageable, resistances between the voltage  
18 source and respective inputs of the differential amplifier, the second  
19 resistances respectively having smaller resistance values than the first  
20 resistances, the second resistances being engaged then disengaged in  
21 response to the voltage source being engaged.  
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1           254. An amplifier in accordance with claim 253 and further  
2 comprising coupling capacitors respectively coupled to the first and  
3 second inputs.  
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5           255. An amplifier in accordance with claim 253 and further  
6 comprising a voltage divider, and wherein the first and second resistances  
7 are coupled to the voltage source via the voltage divider.  
8

9           256. An amplifier in accordance with claim 253 wherein the first  
10 resistances comprise respective transistors.  
11

12           257. An amplifier in accordance with claim 253 wherein the first  
13 resistances comprise respective p-type transistors.  
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15           258. An amplifier in accordance with claim 253 wherein the  
16 second resistances comprise respective transistors.  
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18           259. An amplifier in accordance with claim 253 wherein the  
19 second resistances comprise respective p-type transistors.  
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1 260. A method of speeding power up of an amplifier stage  
2 configured to be powered by a voltage source and including a differential  
3 amplifier having first and second inputs configured to receive an input  
4 signal to be amplified, and having an output; and resistances between the  
5 voltage source and respective inputs of the differential amplifier, the  
6 method comprising:

7 shorting around the selectively resistances for an amount of time  
8 in response to the voltage source being engaged.  
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10 261. A method in accordance with claim 260 wherein the shorting  
11 comprises engaging selectively engageable second resistances respectively  
12 coupled in parallel with the first mentioned resistances and having  
13 respective resistance values lower than the first mentioned resistances.  
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1 262. A method of speeding power up of an amplifier stage  
2 configured to be powered by a voltage source and including first and  
3 second electrodes configured to receive an input signal to be amplified,  
4 the input electrodes being adapted to be respectively coupled to coupling  
5 capacitors; a differential amplifier having inputs respectively connected to  
6 the first and second electrodes, and having an output; and resistances  
7 between the voltage source and respective inputs of the differential  
8 amplifier, the method comprising:

9 shorting around the resistances for a predetermined amount of time  
10 in response to the voltage source being engaged, the shorting comprising  
11 engaging selectively engageable second resistances respectively coupled in  
12 parallel with the first mentioned resistances and having respective  
13 resistance values lower than the first mentioned resistances.  
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1 263. A receiver comprising:

2 a Schottky diode detector;

3 an amplifier coupled to the Schottky diode detector and configured  
4 to be powered by a selectively engageable voltage source, the amplifier  
5 including:

6 a differential amplifier having first and second inputs coupled  
7 to the Schottky diode detector to amplify a signal generated by the  
8 Schottky diode detector, and having an output;

9 first resistances between the voltage source and respective  
10 inputs of the differential amplifier; and

11 second, selectively engageable, resistances between the voltage  
12 source and respective inputs of the differential amplifier, the second  
13 resistances respectively having smaller resistance values than the first  
14 resistances, the second resistances being engaged then disengaged in  
15 response to the voltage source being engaged.

16  
17 264. A receiver in accordance with claim 263 and further  
18 comprising coupling capacitors respectively coupled between the Schottky  
19 diode detector and the first and second inputs of the differential  
20 amplifier.  
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1 265. A receiver in accordance with claim 263 wherein the  
2 amplifier further comprises a voltage divider, and wherein the first  
3 mentioned and second resistances are coupled to the voltage source via  
4 the voltage divider.

5  
6 266. A receiver in accordance with claim 263 wherein the first  
7 mentioned resistances of the amplifier comprise respective transistors.

8  
9 267. A receiver in accordance with claim 263 wherein the first  
10 mentioned resistances of the amplifier comprise respective p-type  
11 transistors.

12  
13 268. A receiver in accordance with claim 263 wherein the second  
14 resistances of the amplifier comprise respective transistors.

15  
16 269. A receiver in accordance with claim 263 wherein the second  
17 resistances comprise respective p-type transistors.

1 270. A method of speeding power-up of an amplifier stage of a  
2 receiver having a Schottky diode detector, the amplifier stage being  
3 configured to be powered by a voltage source and including a differential  
4 amplifier having first and second inputs configured to receive an input  
5 signal to be amplified from the Schottky diode detector, and having an  
6 output; and selectively resistances between the voltage source and  
7 respective inputs of the differential amplifier, the method comprising:

8 shorting around the resistances for an amount of time in response  
9 to the voltage source being engaged.  
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11 271. A method in accordance with claim 270 wherein the shorting  
12 comprises engaging selectively engageable second resistances respectively  
13 coupled in parallel with the first mentioned resistances and having  
14 respective resistance values lower than the first mentioned resistances.  
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272. A method of speeding power up of an amplifier stage of a receiver having a Schottky diode detector, the amplifier stage being configured to be powered by a voltage source and including first and second electrodes configured to receive an input signal to be amplified, the input electrodes being adapted to be respectively coupled to the Schottky diode detector by coupling capacitors to amplify a signal generated by the Schottky diode detector; the amplifier stage further including a differential amplifier having inputs respectively connected to the first and second electrodes, and having an output; and selectively engageable resistances between the voltage source and respective inputs of the differential amplifier, the method comprising:

shorting around the selectively engageable resistances for a predetermined amount of time in response to the voltage source being engaged, the shorting comprising engaging selectively engageable second resistances respectively coupled in parallel with the first mentioned resistances and having respective resistance values lower than the first mentioned resistances.



1        ~~273.~~ A receiver comprising:

2            an RF detector;

3            an amplifier coupled to the RF detector and configured to be  
4        powered by a selectively engageable voltage source, the amplifier  
5        including:

6            a differential amplifier having first and second inputs coupled  
7        to the Schottky diode detector to amplify a signal generated by the  
8        Schottky diode detector, and having an output;

9            first resistances between the voltage source and respective  
10        inputs of the differential amplifier; and

11           second, selectively engageable, resistances between the voltage  
12        source and respective inputs of the differential amplifier, the second  
13        resistances respectively having smaller resistance values than the first  
14        resistances, the second resistances being engaged then disengaged in  
15        response to the voltage source being engaged.

16  
17        274. A receiver in accordance with claim 273 wherein the RF  
18        detector comprises a Schottky diode detector.

19  
20        275. A receiver in accordance with claim 273 wherein the second  
21        resistances comprise transistors.  
22  
23

1        ~~276.~~ An amplifier configured to be powered by a selectively  
2 engageable voltage source, the amplifier comprising:

3            a differential amplifier having first and second inputs for receiving  
4 an input signal to be amplified, and having an output;

5            a first resistance between the voltage source and the first input of  
6 the differential amplifier;

7            a second resistance between the voltage source and the second  
8 input of the differential amplifier;

9            a third, selectively engageable, resistance between the voltage  
10 source and the first input of the differential amplifier, the third  
11 resistance having a smaller resistance value than the first resistance; and

12           a fourth, selectively engageable, resistance between the voltage  
13 source and the first input of the differential amplifier, the fourth  
14 resistance having a smaller resistance value than the first resistance, the  
15 third and fourth resistances being engaged then disengaged in response  
16 to the voltage source being engaged.

17  
18        277. An amplifier in accordance with claim 276 wherein the third  
19 and fourth resistances are simultaneously engaged then disengaged in  
20 response to the voltage source being engaged.

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22        278. An amplifier in accordance with claim 276 wherein the first  
23 resistance comprises a transistor.

1 279. An amplifier in accordance with claim 278 wherein the  
2 second resistance comprises a transistor.

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4 280. An amplifier in accordance with claim 276 wherein the third  
5 resistance comprises a transistor.

6  
7 281. An amplifier in accordance with claim 280 wherein the fourth  
8 resistance comprises a transistor.

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10 ~~282.~~ A method of speeding power up of an amplifier stage  
11 configured to be powered by a voltage source and including a differential  
12 amplifier having first and second inputs configured to receive an input  
13 signal to be amplified, and having an output, a first resistance between  
14 the voltage source and the first input of the differential amplifier, and  
15 a second resistance between the voltage source and the second input of  
16 the differential amplifier, the method comprising:

17 simultaneously shorting around the first and second resistances for  
18 an amount of time in response to the voltage source being engaged.

1 283. An amplifier configured to be powered by a selectively  
2 engageable voltage source, the amplifier comprising:

3 a differential amplifier having first and second inputs for receiving  
4 an input signal to be amplified, and having an output;

5 a first resistance between the voltage source and the first input of  
6 the differential amplifier;

7 a second resistance between the voltage source and the second  
8 input of the differential amplifier;

9 circuitry configured to switch around the third and fourth  
10 resistances for a predetermined amount of time, to cause the inputs to  
11 the differential amplifier to come up to a bias voltage more quickly, in  
12 response to the voltage source being engaged.

13  
14 284. An amplifier in accordance with claim 283 wherein the  
15 circuitry configured to switch around the third and fourth resistances  
16 comprises respective transistors.

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18 285. An amplifier in accordance with claim 284 wherein the first  
19 resistance comprises a transistor.

20  
21 286. An amplifier in accordance with claim 285 wherein the  
22 second resistance comprises a transistor.  
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287. A method of speeding power up of an amplifier stage configured to be powered by a voltage source and including a differential amplifier having first and second inputs configured to receive an input signal to be amplified, and having an output, a first resistance between the voltage source and the first input of the differential amplifier, and a second resistance between the voltage source and the second input of the differential amplifier, the method comprising:

simultaneously switching around the first and second resistances for a predetermined amount of time in response to the voltage source being engaged.--